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Docket No.: Z&PINFP08190

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Giuseppe Curello et al.
Applic. No. : 09/904,360 Confirmation No. 1413
Filed : July 12, 2001

Title : Process for Producing a Doped Semiconductor Substrate

Examiner : Igwe U. Anya
Group Art Unit : 2825
Docket No. : Z&PINFP08190
Customer No. : 24131

DECLARATION under 37 C.F.R. § 1.131

The undersigned Giuseppe Curello and Jürgen Faul hereby declare:

The invention of the above-identified application was "conceived" and "reduced to practice" at least as early as July 4, 2000.

Enclosed, as corroborating evidence is the Invention Disclosure (*Erfindungsmeldung*) filled-out and signed by the undersigned. The Invention Disclosure was executed by the undersigned on July 6, 1999. The Invention Disclosure was given to the Siemens Patent Department on July 9, 1999.

The undersigned declares that all statements made herein of their own knowledge are true and that all statements made on information and belief are believed to be true; and further that

these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and such willful false statements may jeopardize the validity of the application or any patent issued thereon.

_____

Giuseppe Curello

Date: _____, 2004.

_____

Jürgen Faul

Date: _____, 2004.

Vertraulich!
An
Siemens AG
bzw. Beteiligungsgesellschaft

ERFINDUNGSMELDUNG

Bitte verschlossen weitersenden!

Bereits vorab an ZT PA übermittelt per FAX ☐
Wenn ja - bitte unbedingt ankreuzen!

Aktenzeichen der PA: 99 E 5069 DE

Ich/Wir (Vor- und Nachname des/der Erfinder[s] - weitere Angaben und Unterschrift[en] letzte Seite): DR. GIUSEPPE CURELLO; DR. JUERGEN FAUL

Anzahl der Erfinder:

Datum der Ausfertigung:

melde[n] hiermit die auf den folgenden Seiten vollständig beschriebene Erfindung mit der Bezeichnung:

BURIED / RETRO GRADE CHANNEL DOPING PROFILE FABRICATION FOR ADVANCED CMOS IN INTEGRATED CIRCUITS.

I. An Vorgesetzten der/des Erfinder[s]

Herrn/Frau J. FAUL HL DD TE MP (Dienststelle)

mit der Bitte, die nachstehenden Fragen zu beantworten:

a) Wann ging die Erfindungsmeldung bei Ihnen ein? → 6.7.99

b) Geht die Erfindung auf öffentlich geförderte Arbeiten zurück?

☒ nein ☐ ja, Vorhaben:

) Gibt es ein zugehöriges internes FuE-Projekt?

☒ nein ☒ ja, Projekt: [redacted]

Eingang am:

Ab Eingang läuft gesetzliche Frist!

Nur bei ZT-Erfindungen auszufüllen:

Projekt-Nr. _____ Titel: _____ Kerntechnologie: _____

☐ Entwicklungsprojekt ☐ Forschungsprojekt im Interesse von Bereich: _____ Ansprechpartner: _____

d) Anmeldung wird empfohlen ☐ nein ☒ ja

Dringlichkeitsvermerk

Kosten trägt (Organisationseinheit): GG6

☐ Die Erfindung betrifft nicht unser Interessengebiet. Es sind noch folgende Dienststellen zu befragen: _____

6.7.99 (Datum) — (Unterschrift des Vorgesetzten)

Fröhlich - Schötz
06. Juli 1999

II.a Die Erfindungsmeldung bitte an das Referat Ideenmanagement weiterleiten!

Eingang am: 99/07/07

II.b

An das
Referat Ideenmanagement
ATP – Container / Raum: 306

Dresden

ZT GG VM Mch
Eing. 28. JUNI 1999
GR

Eingang am:

Hummer
09.07.99

HRG
HL GG6 DD

1. Welches technische Problem soll durch Ihre Erfindung gelöst werden?
2. Wie wurde dieses Problem bisher gelöst?
3. In welcher Weise löst Ihre Erfindung das angegebene technische Problem (geben Sie Vorteile an)?
4. Worin liegt der erfinderische Schritt?
5. Ausführungsbeispiel(e) der Erfindung.

6. Zur weiteren Erläuterung sind als Anlagen beigefügt:

1 Blatt der Darstellung eines oder mehrerer Ausführungsbeispiele der Erfindung;
(falls möglich, Zeichnungen im PowerPoint- oder Designer-Format anfertigen)

_____ Blatt zusätzliche Beschreibungen (z.B. Laborberichte, Versuchsprotokolle);

_____ Blatt Literatur, die den Stand der Technik, von dem die Erfindung ausgeht, beschreibt; *)

_____ sonstige Unterlagen (z.B. Disketten, insbesondere mit Zeichnungen der Ausführungsbeispiele):

*) Bitte Fotokopien oder Sonderdrucke aller zitierten Veröffentlichungen (Aufsätze vollständig; bei Büchern die relevanten Kapitel) mit vollständigen bibliographischen Daten beifügen.

1) Technisches_Problem
Over the past decad s conventi nal scaling of gate oxide thickness, source / drain extentions, jutiction depth and gate lengths have enabled MOS transistors to be currently mass produced with gate dimensions f 0.2µm and below. Experimental and simulation data show that despite junction depth scaling is still possible (to some extent), increased resistance results in performance degradation so that MOS transistor limits will likely be reached for 0.13 µm process technologies [1].
Because of these limits, it will not be possible to further improve short channel effects (SCE) and this will result in unaccetable off-state leakage currents. Because of this problems now device architectures are being developed for continued transistor scaling. Among the other approaches, the use of retrogade channel doping profile (RCP) for suppressing SCE has been considered and experimentally demonstrated.

2) Bisherige_Problemlösung
The RCP is typically created by using a slow diffusing dopant species such as As or Sb for PMOS and In for NMOS. Recent investigations have shown that an ideal pulse shape doping profile (highly doped region sandwiched between two lighty doped regions) would provide even better transistor performance in the deep-submicrometer regime [2].

For NMOS the use of In (desired also to achieve low Vt NFET and better Vt control) has however been found have some difficulties because of segregation behaviour to the gate oxide and anomalous diffusion and deactivation [3] which will eventually degrade the original retrograde implanted profile. In Dual Gate Oxide processes (used for example in latest eDRAM products) Nitrogen implant is normally used in order to reduce the oxidation rate in selective areas. This Nitrogen implant has also been found to enhance the diffusion of In [EFK Internal communication] aggravating the problem.

In order to fabricate a steep or pulse shape doping channel profile selective epitaxy of undoped Si by the use of UHV-CVD (Ultra High Vacuum Chemical Vapour Deposition) performed following channel implant has been investigated [4, 5] as well as epitaxy of P doped epitaxy [6]. Such epitaxy methods despite being able to achieve steeper doping profile than conventional retrogade channels and improved transistor performance are not practical / mature for a volume production enviroment where high troughput and repeatibility is mandatory.

3) Neuer_Lösungsansatz
The novel method proposed here is to use standard Low Pressure-CVD for the deposition of an undoped thin (20-40 nm) Poly/α -Si (Polycrystalline or Amorphous Silicon) layer following heavy ions retrogade channel implant. The Poly/α -Si deposition can be performed simultaneously for both NMOS and PMOS following patterned well and channel implants. The deposition temperature will determine the Poly grain size and low temperatures (≈ 500-550 C) are preferable in order to achieve a very small average grain size or even better an amorphous layer. After Poly/α -Si deposition, two routes can be undertaken in order to restore the crystal quality of the channel and achieve a clean and planar crystal surface for subsequent gate oxide growth:
   a) Ge+ post amorphization of the whole structure up to a depth (of about 0.5 –1 µm) where end of range defects will be remote from current paths followed by solid phase epitaxy (SPE) by low temperature anneal (≈ 650 C) in order to epitaxially regrow the amorphized layer up to the free surface [7]. A wet etch process could be used to remove any surface oxide formed during such SPE and would also help in improving the Silicon surface quality before the subsequent gate oxidation process. The Ge+ implant is expected to destroy the very thin native oxide which will probably be present at the interface between the deposited Poly/α -Si layer and the implanted substrate. Any residual oxide agglomerate is expected however not to be critical since will be located at the periphery of the channel current path.
   b) RTA (Rapid Thermal Annealing) step performed to break the native oxide interface layer (early mentioned) in sub-nanometer oxide beads while manteining the as implanted profile followed by by low temperature anneal in order to epitaxially regrow the Poly/α -Si layer

up to the free surface. This last process has also been successfully demonstrated in bipolar transistor technology [8]. Similarly to the method a) a wet etch process following the RTA step can be used f r improving th Silicon surface quality before th subsequent gate oxidation process.

4) Erfinderische_Schritt
The proposed process approach described above is able to reproduce steep retrogade channel doping profiles required for advanced CMOS. The complexity of Si epitaxy is avoided by the use of conventional Low Pressure CVD in combination with conventional ion implantation and thermal annealing and is expected to yield comparable performance to epitaxy structures while achieving much superior acceptance in volume production enviroments.

References

[1] Scott Thompson et al. - *MOS Scaling: Transistor Challenges for the 21st Century* - Intel Technology Journal Q3 98.

[2] R.H. Yan et al. - *Scaling the Si MOSFET: From Bulk to SOI to Bulk* - IEEE T. Electr. Dev. Vol. 39, No 7 pag.1704, July 1992.

[3] P. Bouillon et al. - *Anomalous short channel effects in Indium implanted nMOSFETs* - IEDM 97 Techn Digest, pag 897, 1995.

[4] K. Noda et al. - *0.1μm Delta-doped MOSFET Using Post Low-energy Implanting Selective Epitaxy* - Digest of VLSI 94 Techn Symp. pag.19 3A.2, 1994.

[5] T. Skotnicki - *Advanced Architectures for 0.18-0.12 μm CMOS Generations* - Proceedings ESSDERC 96 pag. 505, 1996.

[6] A. Hori et al. - IEDM 93 Techn Digest, pag 19, 1993.

[7] G.Curello et al.- *Beam-power heating effect on the synthesis of graded composition epitaxial Si_1-xGe_x alloy layers.* Nuclear Instruments and Methods in Physics Research B (Beam Interaction with Materials & Atoms) 129, pag. 377, 1997.

[8] F. Priolo et al. - *Interface evolution and epitaxial realignment in polycrystal / single crystal Si structures* - Nuclear Instruments and Methods in Physics Research B (Beam Interaction with Materials & Atoms) 85 pag. 159, 1994.

Ausführungsbeispiele